ABSTRACT OF THE DISCLOSURE

In a semiconductor memory device, a precharge potential for non-selected bit lines among a plurality of bit lines, supplied by a HPR voltage source, is set at a value (for example, 1/2 Vcc = 0.4 V) lower than the power supply voltage Vcc (low voltage in the range of 0.5 V to 1.2 V; for example, 0.8 V) determining the high-level side potential of data stored in a memory cell. A potential for non-selected word lines among a plurality of word lines, supplied by a NWL voltage source, is set at a predetermined negative potential (for example, -1/4 Vcc = -0.2 V). The total of the precharge potential (0.4 V) of non-selected bit lines and the absolute value of the negative potential (-0.2 V) of non-selected word lines is set at a value less than the power supply voltage Vcc (0.8 V). By these settings, gate leakage current and GIDL current can be effectively limited to a small value while realizing effective limitation of OFF leakage current in a plurality of memory cells.